ABSTRACT OF THE DISCLOSURE

A semiconductor memory device, which can hides a delay in a refresh operation from an outside for speeding up operation, comprises a memory cell including first and second transistors connected between a bit line for a write system and a bit line for a read system, and a capacitor C for data storage, in which a word line for a write system and a word line for a read system are connected to control terminals of the two transistors, respectively, a circuit for comparing a refresh address with an address selected according to a read/write signal among read/write addresses from an address holding circuit for holding input address signal and performing control so that if a mismatch is detected, a read/write operation using one of the read and write systems, selected by the read or write address and a refresh operation using the other of the read and write systems, selected by the refresh address are performed in parallel and if a match has been detected, the read or write operation using the word line and the bit line associated with one of the read and write systems is performed.